2613

TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. EN998073

In Re Application Of: **Greenfield et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/186,584	11/05/98	Richard J. Lee	2613

Invention: **ON-CHIP DYNAMIC BUFFER LEVEL INDICATORS FOR DIGITAL VIDEO ENCODER**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **December 16, 2002**

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A duplicate copy of this sheet is enclosed.

Kevin P. Radigan
Signature

Dated: **January 09, 2003**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Greenfield et al.	:	Group Art Unit: 2613
Serial No.: 09/186,584	:	Examiner: Richard J. Lee
Filed: November 5, 1998	:	Appeal No.:

For: ON-CHIP DYNAMIC BUFFER LEVEL INDICATORS
FOR DIGITAL VIDEO ENCODER

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Board of Patent Appeals and Interferences
Assistant Commissioner for Patents
Washington, D.C. 20231

Brief of Appellants

Dear Sir:

This is an appeal from a final rejection, dated September 18, 2002, rejecting claims 1-35, all the claims being considered in the above-identified application. This Brief is accompanied by a transmittal letter authorizing the charging of appellants' deposit account for payment of the requisite fee set forth in 37 C.F.R. §1.17(c).

Real Party In Interest

This application is assigned to **International Business Machines Corporation** by virtue of an assignment executed on November 4, 1998 by the co-inventors and recorded with the United States Patent and Trademark Office at reel 9571, frame 0724, on November 5, 1998. Therefore, the real party in interest is **International Business Machines Corporation**.

Related Appeals and Interferences

To the knowledge of the appellants, appellants' undersigned legal representative, and the assignee, there are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the instant appeal.

Status of Claims

This patent application was filed on November 5, 1998 with the United States Patent and Trademark Office. As filed, the application included thirty-one (31) claims, of which four (4) were independent claims (i.e., claims 1, 9, 16 & 27).

In an initial Office Action dated January 25, 2001, claims 1-31 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention; claims 1-6 & 16-19 were rejected under 35 U.S.C. §102(e) as being anticipated by Greenfield et al. (U.S. Patent No. 5,760,836; hereinafter, "Greenfield"); claims 7-15 & 20-31 were rejected under 35 U.S.C. §103(a) as being unpatentable over Greenfield as applied to claims 1-6 & 16-19, and further in view of Choe et al. (U.S. Patent No. 6,094,696; hereinafter, "Choe"). In appellants' response dated April 24, 2001, claims 1-3, 6, 9-13, 17-19, 21, 22, 24, 27 & 29 were amended.

In a second and final Office Action dated July 13, 2001, claims 1-6 & 16-19 were rejected under 35 U.S.C. §102(e), as being anticipated by Greenfield; while claims 7-15 & 20-31 were rejected under 35 U.S.C. §103(a) as being unpatentable over Greenfield as applied to claims 1-6 & 16-19, and further in view of Choe. In appellants' response dated September 13, 2001, claims 1, 2, 9, 16, 17 & 27 were amended and new claims 32-35 were added.

Appellants received an Advisory Action dated September 21, 2001, which indicated that appellants' Response to the final Office Action raised new issues. These unentered amendments were subsequently entered through a continued prosecution application (CPA), which appellants filed under 37 C.F.R. §1.53(d) on October 12, 2001.

In a non-final Office Action dated April 8, 2002, claims 1-6, 16-19, 32 & 34 were rejected under 35 U.S.C. §102(e), as being anticipated by Greenfield; while claims 7-15, 20-31, 33 & 35 were rejected under 35 U.S.C. §103(a) as being unpatentable over Greenfield as applied to claims 1-6, 16-19, 32 & 34, and further in view of Choe. In appellants' response dated July 2, 2002, claims 1, 2, 9, 16, 17, 27 & 32-35 were amended.

In a final Office Action mailed September 18, 2002, claims 1-6, 16-19, 32 & 34 were again rejected under 35 U.S.C. §102(e), as being anticipated by Greenfield; while claims 7-15, 20-31, 33 & 35 were rejected under 35 U.S.C. §103(a) as being unpatentable over Greenfield as applied to claims 1-6, 16-19, 32 & 34, and further in view of Choe. Appellants' response dated November 18, 2002 included no claim amendments and was accompanied by a Declaration by co-inventor Agnes Y. Ngai (filed under 37 C.F.R. §1.132) in support of the novelty and non-obviousness of the pending claims.

Appellants received an Advisory Action dated December 4, 2002, which indicated that the appellants' Response to the final Office Action did not place the application in condition for allowance.

A Notice of Appeal to the Board of Patent Appeals and Interferences was filed on December 16, 2002. The status of the claims is therefore as follows:

Claims allowed - none;
Claims objected to - none;
Claims rejected - 1-35; and
Claims canceled - none.

Appellants are appealing the rejection of claims 1-35.

Status of Amendments

Appellants' remarks proffered in the Response to the final Office Action dated September 18, 2002 were entered upon filing of the Notice of Appeal and this Appeal Brief. However, no claim amendment was effectuated by the Response. The claims as set out in Appendix A include all prior entered amendments.

Summary of the Invention

Appellants' invention is a particular technique (e.g., claim 1) for encoding a digital video image stream in an encoder 11 (FIG. 1), including spatial compression of still images in the digital video image stream and temporal compression between the still images. The spatial compression is carried out by converting a time domain image of a macroblock (FIG. 4) to a frequency domain image of the macroblock, taking a discrete cosine transform 21 (FIG. 1) of the frequency domain image, transforming the discrete cosine transformed macroblock image by a quantization factor 23 (FIG. 1), and run length encoding 25 (FIG. 1) the quantized discrete cosine transformed macroblock image. Further, the temporal compression is carried out by reconstructing (see 131, 29, 31 of FIG. 1) the quantized, discrete cosine transformed image of the macroblock, searching for a best match macroblock (42 to 43, FIG. 1), and constructing a motion vector 113

(FIG. 1) therebetween. In these ways, the spatial compression and temporal compression form a bitstream including run length encoded, quantized, discrete cosine transformed macroblocks and motion vectors, and pass the bitstream to and through an external buffer 51 (FIG. 1) to a transmission medium. The technique's improvement includes feeding back to hardware logic within the encoder 200 (FIG. 5) an external buffer read signal from a host FIFO_RD and incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (R) (FIG. 5), and determining the number of bits encoded and written into an external buffer (E) (FIG. 5), and in the hardware logic of the encoder subtracting from the number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the fullness 220 (FIG. 5) of an external buffer 201 (FIG. 5), and providing, from the hardware logic within the encoder to the host, a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF) 240 (FIG. 5). See also specification, page 16 line 5 – page 17, line 32.

In another aspect, the invention includes the technique for encoding a digital video image stream described above with the improvement further including providing, from the hardware logic within the encoder to the host, in real time a dynamically updated flag comprising at least one of a BUFFER_EMPTY flag, BUFFER_ALMOST_FULL flag and a BUFFER_FULL flag (e.g., claim 9; see also specification, page 20, line 7 – page 21, line 2 and 340, 350 & 370 of FIG. 6).

In a further aspect, the continuously obtaining of the external buffer fullness includes obtaining the external buffer fullness every cycle of the encoder (e.g., claims 32-35; see specification, page 17, lines 1-7 and page 19, lines 19-27).

Issues

1. Whether claims 1-6, 16-19, 32 & 34 were anticipated under 35 U.S.C. §102(e) by Greenfield (U.S. Patent No. 5,760,836).

2. Whether claims 7-15, 20-31, 33 & 35 were rendered obvious under 35 U.S.C. §103(a) over Greenfield as applied to claims 1-6, 16-19, 32 & 34, and further in view of Choe (U.S. Patent No. 6,094,696).

Grouping of Claims

Since each ground of rejection provides a group of claims, the following groups of claims are included herein:

I. Claims 1-6, 16-19, 32 & 34; and

II. Claims 7-15, 20-31, 33 & 35.

As understood, the claims of one group of claims do not stand or fall with any other groups of claims. Rather, each group of claims is decided independently of the other groups of claims.

Additionally, appellants respectfully submit that claims of Group I do not stand or fall together. For example, claims 32 & 34 include additional features that provide a separate basis of patentability.

Moreover, appellants respectfully submit that the claims of Group II do not stand or fall together. For example, claims 33 & 35 include additional features that provide a separate basis of patentability.

Argument

Group I: Claims 1-6, 16-19, 32 & 34

Claims 1-6, 16-19, 32 & 34 stand rejected under 35 U.S.C. §102(e) as being anticipated by Greenfield. Appellants respectfully request reversal of this rejection.

In independent claims 1 & 16, appellants recite a technique for encoding a digital video image stream in an encoder. The technique includes feeding back to hardware logic within the encoder an external buffer read signal from a host and incrementing an on-chip counter of the hardware logic each time that the external buffer is read, and counting therefrom the number of bits read by a host (R). The technique further includes determining the number of bits encoded and written into an external buffer (E), and in hardware logic of the encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the fullness of an external buffer (BF). The technique further includes providing, from the hardware logic of the encoder to the host, a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF).

The present invention thus employs hardware to continuously monitor the real time fullness of the external buffer and provide a dynamic buffer level indicator indicative of the fullness of the external buffer. This dynamic buffer level indicator assists the host's application in the control of reading compressed data from the external buffer coupled to the encoder. The buffer level indicator is dynamic in that the indicator is adjusted based on continuous monitoring of the external buffer, e.g., every machine cycle of the encoder (see specification, page 4, lines 26-33).

In support of the anticipation rejection, the final Office Action alleged that the teachings at columns 5-7 of Greenfield recite the above-summarized aspects of appellants' invention. This characterization of the teachings of Greenfield is respectfully

traversed. In support of this traversal and the following comments, appellants note the significant overlapping in inventorship between the present application and the inventors of the Greenfield patent. Agnes Y. Ngai, co-inventor of the present invention and co-inventor on the Greenfield patent, has provided a characterization of the teachings and capabilities of the Greenfield system which supports the differences discussed below with respect to that system (see 37 C.F.R. §1.132 Declaration of Agnes Y. Ngai enclosed with the November 18, 2002 Response to Final Office Action, and attached hereto as Appendix B).

Appellants respectfully submit that a careful reading of Greenfield fails to uncover any teaching, suggestion or implication that the processing or logic described therein comprises a dynamic buffer level indicator that is provided as recited by appellants herein. In fact, Greenfield specifically describes a non-real time buffer level indicator. In Greenfield, the buffer level indicator is provided dependent upon how often the processor updates the indicator. The hardware described in Greenfield would be incapable of supporting a continuously obtaining application as recited herein. Column 6, lines 18-29 specifically state that the microcode reads the register and compares it with the buffer fullness in bytes (BF/8). Also, column 5, lines 50-57 indicate that the microcode reads a counter and the FIFO configuration register, and then calculates the amount of data read by the host (R), which is used to calculate the fullness of the external buffer (see also Ngai Declaration, page 2, line 25 – page 3, line 8). Since Greenfield's microcode-based buffer fullness calculation includes a sequence of instructions, the buffer fullness that is known at the end of processing this sequence of instructions is not known during the processing of the sequence. In other words, while the processor is doing the updating of the buffer level indicator, the buffer level signal is not returned on a continuous basis. As one example, in the Greenfield system, a buffer level indicator would be returned approximately once per macroblock or picture frame (column 6, lines 9-11; see also Ngai Declaration, page 3, lines 17-18). In contrast, appellants' hardware logic continuously obtains the fullness of the external buffer (e.g., claim 1).

Appellants' specification notes that the disadvantage of the above-summarized approach (i.e., the Greenfield approach) is that it is implemented in microcode, and therefore, buffer fullness in not constantly monitored (specification, page 14, line 31 – page 15, line 2). Without a continuous view of the fullness of the buffer, the host processor must wait until the microcode goes in, polls the on-chip register and calculates the fullness of the FIFO. This creates a latency issue which produces an inherent inaccuracy in the FIFO fullness reading (specification, page 15, lines 2-7). Appellants wish to emphasize that the present invention arose from appellants' identifying of the deficiency of the Greenfield teachings in this respect.

The present invention solves this problem by implementing FIFO monitoring and a dynamic FIFO buffer level indicator in hardware logic inside the digital video encoder for interfacing, for example, to an industry standard FIFO buffer or cascaded FIFO buffers. Thus, appellants continuously attain the recited dynamic buffer level indicator through the use of a hardware implementation (specification, page 15, lines 7-16). As noted above, Greenfield describes a microcode implementation, which, based on the processing described therein, comprises a non-continuous implementation. This is understood by one skilled in the art through the use of a non-real time counter to monitor the amount of data written to the FIFOs in Greenfield (see column 6, lines 10-11), and through the use of a non-continuous sampling of this counter by the microcode.

In response to the Examiner's comments contained in paragraph 5 at pages 6-9 of the final Office Action, appellants note that column 1, lines 32-49, column 5, lines 24-30 & 53-67, and columns 6 & 7 all discuss a real time encoder. However, these columns do not teach, suggest or imply continuous monitoring of external buffer fullness, as recited in appellants' independent claims. As discussed in the Ngai Declaration at page 2, lines 17-24, Greenfield's real time encoding system means that the encoder therein is capable of completing calculations necessary to encode pictures at a rate specified by a relevant standard (e.g., thirty frames per second under the NTSC standard). Thus the "real time"

aspect of Greenfield's system is different from and independent of appellants' recited continuous monitoring of external buffer fullness.

In paragraph 5 of the final Office Action, the Examiner cites column 5, lines 24-30 & 53-67 of Greenfield as indicating that the fullness of an external buffer is continuously obtained through hardware logic in the encoder adapted to monitor the number of bits encoded and make calculations using the number of bits read by the host (page 7, lines 5-9). Although Greenfield describes a microcode process that monitors the number of bits encoded and calculates external buffer fullness, it does not follow that buffer fullness is constantly available through continuous monitoring. The Ngai Declaration clearly establishes that the Greenfield system does not provide any means to continuously obtain the fullness of the external buffer, and one skilled in the relevant art would not expect Greenfield's hardware logic to be capable of being modified to continuously obtain buffer fullness (see Ngai Declaration, page 3, lines 9-13). Thus, appellants respectfully traverse the Examiner's conclusion that external buffer fullness is continuously obtained in Greenfield.

In view of the above, appellants respectfully submit that there are clear differences between the encoding technique recited in claims 1 & 16 and the teachings, suggestions or implications in Greenfield. Therefore, appellants request withdrawal of the anticipation rejection and allowance of independent claims 1 & 16, as well as the claims which depend therefrom.

In addition to the above, claims 32 & 34 have a separate basis of patentability. For example, these claims further recite that the continuous obtaining includes obtaining the fullness of the external buffer (BF) every cycle of the encoder. This continuous obtaining of the external buffer fullness every encoder cycle is quite different from Greenfield's buffer indicator. As noted above, Greenfield explicitly describes a non-real time buffer level indicator calculated by microcode. Since the buffer fullness calculation includes a sequence of instructions, and only one instruction may be, for instance,

executed per encoder cycle, the microcode cannot perform the buffer fullness calculation every encoder cycle (see Ngai Declaration, page 3, line 6). Thus, in Greenfield, the actual fullness of the buffer is not continuously obtained every cycle, as recited in the present invention.

Based on the foregoing, appellants respectfully request reversal of the §102 rejection of the claims of Group I.

Group II: Claims 7-15, 20-31, 33 & 35

As noted, claims 7-15, 20-31, 33 & 35 were rejected in the final Office Action as obvious over Greenfield in view of Choe. Appellants respectfully submit that the combination of Greenfield and Choe fails to teach, suggest or imply one or more features recited in the claims of Group II. Thus, appellants request reversal of the §103 rejection as applied to these claims.

Each independent claim at issue (i.e., claims 9 & 27) recites a technique wherein hardware logic within the encoder continuously obtains and provides to the host a dynamically updated flag. Neither Greenfield nor Choe continuously obtain and provide from encoder hardware to a host a dynamically updated flag. In fact, appellants note that Choe does not even involve an encoding process.

As noted above, a careful reading of Greenfield fails to uncover any teaching, suggestion or implication of hardware logic implementing a technique wherein a dynamic buffer level indicator is continuously obtained and provided to a host. Similarly, a careful reading of Choe fails to uncover any discussion of an encode process, let alone the provision of a dynamic buffer level indicator from an encoder to a host. In fact, a careful reading of Choe fails to uncover any dynamic indicator being continuously provided, as disclosed in the present application. Choe discloses a data transfer mechanism where a set of buffer_full and buffer_empty flags are implemented for each device (see column 2, lines 62-67). Once a flag is set, it has to be reset by the CPU. This

is in contrast with the flags disclosed by appellants which are dynamic, real time indicators. As the data is added to the pre-defined full level the buffer_full flag is asserted in appellants' case. Further, as data is removed to below the pre-defined full level, the buffer_full flag is deasserted without any CPU intervention (see specification, page 20, line 27 – page 21, line 2). The flags of Choe are used to start data transfer operations (column 3, lines 3-21). In contrast, the flags recited by appellants do not necessarily initiate data transfer. Appellants' flags are used to regulate the data rate in and out of the FIFOs in a simultaneous and continuous manner.

For all the above reasons, appellants respectfully submit that independent claims 9 & 27 would not have been obvious to one of ordinary skill in the art based upon Greenfield and Choe. In appellants' recited invention, hardware logic within the encoder performs certain functions, including subtracting from a number of bits encoded the number of bits read by the host to continuously obtain the fullness of an external buffer. Further, from this hardware logic, a dynamically updated flag is provided in real time to a host. Since appellants' invention is implemented within hardware logic within the encoder, no CPU intervention is required. In fact, only with a hardware implementation is it possible to obtain appellants' recited continuously obtaining the fullness of the external buffer and providing in real time the dynamically updated flag.

Further, appellants respectfully submit that claims 33 & 35 have a separate basis of patentability. For example, these claims recite that the hardware logic continuously obtains the fullness of the external buffer every cycle of the encoder. A careful reading of the applied art fails to uncover any suggestion or capability that the systems described therein could obtain the fullness of the external buffer every cycle of the encoder. In fact, this is simply not possible using a CPU based system such as described by Greenfield and Choe.

For all of the above reasons, appellants respectfully request reversal of the §103 rejection of the claims in Group II.

Conclusion

Appellants respectfully request reversal of each of the rejections set forth in the final Office Action. Appellants respectfully submit that their claimed invention is not anticipated by Greenfield, nor is it obvious to one of ordinary skill in the art based upon Greenfield and Choe, either alone or in combination. In support of their position regarding the claims, appellants note that Greenfield does not describe, suggest or imply continuously obtaining the fullness of an external buffer, or providing, from hardware logic, a dynamic buffer level indicator. Greenfield instead describes a non-continuous buffer level indicator that is updated with a frequency dependent upon the microcode. Furthermore, neither Greenfield nor Choe teach or suggest continuously obtaining and providing from encoder hardware a dynamically updated flag. In addition, many of appellants' dependent claims provide further characterizations which are believed absent from the applied art. For example, neither Greenfield nor Choe describe or suggest obtaining the fullness of the external buffer every encoder cycle.

For all of the above reasons, appellants allege error in rejecting their claims as anticipated and/or obvious based on the applied art. Accordingly, reversal of all rejections is respectfully requested.

Respectfully submitted,

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Appendix A

1. In a method of encoding a digital video image stream in an encoder, comprising spatial compression of still images in the digital video image stream and temporal compression between the still images, wherein the spatial compression is carried out by converting a time domain image of a macroblock to a frequency domain image of the macroblock, taking a discrete cosine transform of the frequency domain image, transforming the discrete cosine transformed macroblock image by a quantization factor, and run length encoding the quantized discrete cosine transformed macroblock image, wherein the temporal compression is carried out by reconstructing the quantized, discrete cosine transformed image of the macroblock, searching for a best match macroblock, and constructing a motion vector therebetween, to thereby form a bitstream comprising run length encoded, quantized, discrete cosine transformed macroblocks and motion vectors, and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising feeding back to hardware logic within the encoder an external buffer read signal from a host and incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (R), and determining the number of bits encoded and written into an external buffer (E), and in the hardware logic of the encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the fullness of an external buffer (BF), and providing, from the hardware logic within the encoder to the host, a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF).

2. The method of claim 1, wherein said providing the host with said dynamic buffer level indicator comprises continuously comparing the fullness of the external buffer (BF) with a buffer threshold (BT) defined by said host and providing a high-level indicator when a buffer fullness (BF) is greater than the buffer threshold (BT), and a low-level indicator when the buffer threshold (BT) is greater than the buffer fullness (BF).

3. The method of claim 2, further comprising retaining said buffer threshold (BT) in a register within the encoder for use in comparing of buffer fullness (BF) to the buffer threshold (BT).

4. The method of claim 1, further comprising providing an external buffer configuration register in said encoder for retaining multiple external buffer configuration values, and wherein said calculating in the encoder the number of bits read by the host (R) includes employing a predefined configuration value of the external buffer configuration register in determining the number of bits read by the host (R) upon receipt of each buffer read signal from the host.

5. The method of claim 4, wherein said multiple external buffer configuration values retained in said external buffer configuration register comprise at least some of 1, 2, 4 and 8 byte buffer configuration values, each value being representative of a number of bytes read from said external buffer with each buffer read signal from the host for a respective external buffer configuration.

6. The method of claim 1, wherein said external buffer comprises a FIFO buffer.

7. The method of claim 1, wherein said external buffer comprises one of a field buffer or cascaded FIFO buffers, and wherein said dynamic buffer level indicator comprises at least one of a BUFFER_EMPTY flag, BUFFER_ALMOST_FULL flag and BUFFER_FULL flag.

8. The method of claim 1, wherein said providing the host in real time with said dynamic buffer level indicator comprises providing the host in real time with multiple dynamically updated flags, said multiple dynamically updated flags comprising a BUFFER_EMPTY flag, BUFFER_ALMOST_FULL flag and BUFFER_FULL flag.

9. In a method of encoding a digital video image stream in an encoder, comprising spatial compression of still images in the digital video image stream and temporal compression between the still images, wherein the spatial compression is carried out by converting a time domain image of a macroblock to a frequency domain image of the macroblock, taking a discrete cosine transform of the frequency domain image, transforming the discrete cosine transformed macroblock image by a quantization factor, and run length encoding the quantized discrete cosine transformed macroblock image, wherein the temporal compression is carried out by reconstructing the quantized, discrete cosine transformed image of the macroblock, searching for a best match macroblock, and constructing a motion vector therebetween, to thereby form a bitstream comprising run length encoded, quantized, discrete cosine transformed macroblocks and motion vectors, and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising feeding back to hardware logic within the encoder an external read signal from a host and incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (R), and determining the number of bits encoded and written into an external buffer (E), and in the hardware logic of the encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the fullness of an external buffer (BF), and providing, from the hardware logic within the encoder to the host, in real time a dynamically updated flag comprising at least one of a BUFFER_EMPTY flag, a BUFFER_ALMOST_FULL flag and a BUFFER_FULL flag.

10. The method of claim 9, wherein said providing the host in real time with said dynamically updated flag comprises providing the host in real time with at least said BUFFER_EMPTY flag, said providing of said BUFFER_EMPTY flag comprising continuously determining whether said fullness of the external buffer (BF) is equal to 0, and providing a high-level indicator when a buffer fullness (BF) is 0, and a low-level indicator when the buffer fullness is greater than 0.

11. The method of claim 9, wherein said providing the host in real time with said dynamically updated flag comprises providing the host with at least said BUFFER_ALMOST_FULL flag, said providing of said BUFFER_ALMOST_FULL flag comprising continuously determining whether the fullness of the external buffer (BF) is greater than or equal to a buffer threshold (BT), and providing said host with a high-level indicator when a buffer fullness (BF) is greater than or equal to said buffer threshold (BT), and a low-level indicator when the buffer threshold (BT) is greater than the buffer fullness (BF).

12. The method of claim 11, further comprising providing an on-chip buffer threshold register, said on-chip buffer threshold register containing a host defined buffer threshold value for use in comparing of said buffer fullness (BF) to said buffer threshold (BT).

13. The method of claim 9, wherein said providing the host in real time with said dynamically updated flag comprises providing the host in real time with at least said BUFFER_FULL flag, said providing of said BUFFER_FULL flag, comprising continuously comparing the fullness of the external buffer (BF) to a predefined buffer size (BS), and providing the host with a high-level indicator when a buffer fullness (BF) is greater than or equal to said buffer size (BS), and a low-level indicator when said buffer size (BS) is greater than said buffer fullness (BF).

14. The method of claim 13, further comprising providing an on-chip buffer size register for holding a host-defined buffer size value for use in said comparing of said buffer fullness (BF) to said buffer size (BS).

15. The method of claim 9, wherein said external buffer comprises one of an external field buffer or external cascaded FIFOs.

16. An encoder for encoding a digital video image stream in the encoder, comprising means for spatial compression of still images in the digital video image stream and means for temporal compression between the still images, wherein the means for spatial compression comprises means for converting a time domain image of a macroblock to a frequency domain image of the macroblock, means for taking a discrete cosine transform of the frequency domain image, means for transforming the discrete cosine transformed macroblock image by a quantization factor, and means for run length encoding the quantized discrete cosine transformed macroblock image, wherein the means for temporal compression comprises means for reconstructing the quantized, discrete cosine transformed image of the macroblock, means for searching for a best match macroblock, and means for constructing a motion vector therebetween, said encoder for encoding a digital video image stream thereby forming a bitstream comprising run length encoded, quantized, discrete cosine transform macroblocks and motion vectors and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising means for feeding back to hardware logic within the encoder an external read signal from a host, and for incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (R), said hardware logic in the encoder being further adapted to monitor a number of bits encoded (E) and written into the external buffer and subtract from the number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the fullness of an external buffer (BF), and wherein said hardware logic in the encoder is further adapted to provide the host with a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF).

17. The encoder of claim 16, wherein said logic adapted to provide the host with a dynamic buffer level indicator comprises logic adapted to continuously compare the fullness of the external buffer (BF) with a buffer threshold (BT) defined by said host and to provide a high-level indicator when a buffer fullness (BF) is greater than the buffer

threshold (BT), and a low-level indicator when the buffer threshold (BT) is greater than the buffer fullness (BF).

18. The encoder of claim 17, further comprising a buffer threshold (BT) register within the encoder coupled to said logic adapted to compare said buffer fullness (BF) to the buffer threshold (BT).

19. The encoder of claim 16, wherein said external buffer comprises at least one FIFO buffer.

20. The encoder of claim 16, wherein said external buffer comprises one of a field buffer or cascaded FIFO buffers, and wherein said dynamic buffer level indicator comprises at least one of a BUFFER_EMPTY flag, BUFFER_ALMOST_FULL flag and BUFFER_FULL flag.

21. The encoder of claim 20, wherein said dynamic buffer level indicator comprises said BUFFER_EMPTY flag, and wherein said logic is further adapted to continuously determine whether said fullness of the external buffer (BF) is equal to 0, and provide a high-level indicator when a buffer fullness (BF) is 0, and a low-level indicator when the buffer fullness is greater than 0.

22. The encoder of claim 20, wherein said dynamic buffer level indicator comprises said BUFFER_ALMOST_FULL flag, and wherein said logic is further adapted to continuously determine whether the fullness of the external buffer (BF) is greater than or equal to a buffer threshold (BT), and to provide said host with a high-level indicator when a buffer fullness (BF) is greater than or equal to said buffer threshold (BT), and a low-level indicator when the buffer threshold (BT) is greater than the buffer fullness (BF).

23. The encoder of claim 22, further comprising an on-chip buffer threshold register, said on-chip buffer threshold register containing a host defined buffer threshold value for use by said logic in comparing said buffer fullness (BF) to said buffer threshold.

24. The encoder of claim 20, wherein said dynamic buffer level indicator comprises said BUFFER_FULL flag, and wherein said logic is adapted to continuously compare the fullness of the external buffer (BF) to a predefined buffer size (BS), and to provide the host with a high-level indicator when a buffer fullness (BF) is greater than or equal to said buffer size (BS), and a low-level indicator when said buffer size (BS) is greater than said buffer fullness (BF).

25. The encoder of claim 24, further comprising an on-chip buffer size register within said encoder for holding a host-defined buffer size value for use by said encoder logic in comparing said buffer fullness (BF) to said buffer size (BS).

26. The encoder of claim 20, wherein said external buffer comprises one of an external field buffer or external cascaded FIFOs.

27. An encoder for encoding a digital video image stream in the encoder, comprising means for spatial compression of still images in the digital video image stream and means for temporal compression between the still images, wherein the means for spatial compression comprises means for converting a time domain image of a macroblock to a frequency domain image of the macroblock, means for taking a discrete cosine transform of the frequency domain image, means for transforming the discrete cosine transformed macroblock image by a quantization factor, and means for run length encoding the quantized discrete cosine transformed macroblock image, wherein the means for temporal compression comprises means for reconstructing the quantized, discrete cosine transformed image of the macroblock, means for searching for a best match macroblock, and means for constructing a motion vector therebetween, said means for encoding a digital video image stream thereby forming a bitstream comprising run

length encoded, quantized, discrete cosine transform macroblocks and motion vectors and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising means for feeding back to hardware logic within the encoder an external read signal from a host, and for incrementing an on-chip counter of the hardware logic each time the external buffer is read and calculating therefrom the number of bits read by a host (R), said hardware logic in the encoder being further adapted to monitor a number of bits encoded (E) and written into the external buffer and subtract from the number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the fullness of an external buffer (BF), and wherein said hardware logic in the encoder is further adapted to provide the host in real time with dynamically updated flags comprising a BUFFER_EMPTY flag, a BUFFER_ALMOST_FULL flag and a BUFFER_FULL flag.

28. The encoder of claim 27, wherein said external buffer comprises one of an external field buffer or external cascaded FIFOs.

29. The encoder of claim 28, wherein said logic adapted to provide said BUFFER_EMPTY flag comprises logic adapted to continuously determine whether said fullness of the external buffer (BF) is equal to 0, and to provide a high-level indicator when a buffer fullness (BF) is 0, and a low-level indicator when the buffer fullness is greater than 0.

30. The encoder of claim 29, wherein said logic adapted to provide said BUFFER_ALMOST_FULL flag comprises logic adapted to continuously determine whether the fullness of the external buffer (BF) is greater than or equal to a buffer threshold (BT), and to provide said host with a high-level indicator when the buffer fullness (BF) is greater than or equal to said buffer threshold (BT), and a low-level indicator when the buffer threshold (BT) is greater than the buffer fullness (BF).

31. The encoder of claim 30, wherein said logic adapted to provide said BUFFER_FULL flag comprises logic adapted to continuously compare the fullness of the external buffer (BF) to a predefined buffer size (BS), and to provide the host with a high-level indicator when the buffer fullness (BF) is greater than or equal to said buffer size (BS), and a low-level indicator when said buffer size (BS) is greater than said buffer fullness (BF).

32. The method of claim 1, wherein the continuously obtaining comprises obtaining the fullness of the external buffer (BF) every cycle of the encoder.

33. The method of claim 9, wherein the continuously obtaining comprises obtaining the fullness of the external buffer (BF) every cycle of the encoder.

34. The encoder of claim 16, wherein the hardware logic continuously obtains the fullness of the external buffer (BF) every cycle of the encoder.

35. The encoder of claim 27, wherein the hardware logic continuously obtains the fullness of the external buffer (BF) every cycle of the encoder.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Greenfield et al. Confirmation No.: 1986

Serial No: 09/186,584 Examiner: Lee, Richard J.

Filed: 11/05/98 Group Art Unit: 2613

Title: ON-CHIP DYNAMIC BUFFER LEVEL INDICATORS FOR DIGITAL VIDEO ENCODER

Declaration Under 37 C.F.R. §1.132

TO: Box AF
Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, Agnes Y. Ngai, declare:

1. I reside at 725 Partridge Place, Endwell, New York 13760.

2. I earned a B.S. in Electrical Engineering from the City College of New York in 1973.

3. I have worked for International Business Machines (IBM) Corporation from 1973 to the present. I have worked at IBM's Microelectronics Semiconductor Digital Video Products Group from 1992 to the present. My experience at IBM also includes working in S370 midrange processing technology, RISC processing technology, and memory subsystems. Since 1992 my work has focused on video compression and decompression development.

4. I have authored and co-authored over 40 patents and a number of publications. I am a recipient of the IBM 16th Plateau Invention Achievement Award.

5. As a co-inventor, I have reviewed and do understand the contents of the above–identified application, which is directed, in part, to a novel hardware implementation of certain features of a digital video encoding system. Further, I am a co-inventor of the applied patent issued to Greenfield et al. (U.S. Patent No. 5,760,836) and do understand the contents of that

patent. In addition, I have reviewed the Choe et al. patent (U.S. Patent No. 6,094,696), and am aware of the final Office Action mailed September 18, 2002 in connection with the above-designated application.

In support of the novelty and non-obviousness of the pending claims, I present herewith an explanation of certain features of the Greenfield et al. encoding system, and why the pending claims would not have been anticipated or obvious to myself or other experts in the field based on the applied patents.

For a teaching of my claimed concept, the Office Action relies significantly on the language at column 5, line 24-30 of Greenfield et al. ('836), where it is stated that a real-time encoding system is provided, which is repeated herein for convenience.

> Another factor which can be used to adjust the step size is the fullness of the external buffer, which in real time encoding systems is typically an external FIFO device. By monitoring the amount of data read from the FIFOs and data used to encode the bitstream (E), the bitrate can be adjusted to prevent overflow of the external buffers 51 in a normal operating environment.

The "real-time encoding system" of Greenfield et al. means that the encoder discussed therein is capable of encoding a number of pictures per second as specified by the relevant standard, which in the case of NTSC means 30 frames per second. Depending on the operating frequency of the encoder, there are thousands and thousands of cycles per picture. A real time encoding thus means that the encoder can complete the calculations or executions needed to produce, e.g., thirty frames in one second. I submit as an expert skilled in the art, that this does not mean one would read Greenfield et al. as necessarily inferring that the encoder is executing or performing the same calculation or instruction every cycle.

The method of calculating external buffer fullness disclosed by Greenfield et al. is cited at column 5, lines 50-57 to include reading the counter and FIFO configuration register using microcode. Microcode then performs the R (number of bits read by the host) calculation. The microcode also monitors the number of bits encoded, and subtracts the amount of data read by the host. The result of this calculation is the fullness of the external buffer. This teaching of

Greenfield et al. clearly states that microcode is used to monitor the external buffer fullness. Microcode performs a function, calculation of buffer fullness in this case, by executing a sequence of different instructions. One instruction may be, for instance, executed once per machine cycle. The end of the sequence of instructions produces the desired calculation. Since different instructions are executed each cycle in the sequence needed to calculate or determine buffer fullness, the microcode cannot perform a buffer fullness calculation every cycle. Because the microcode cannot provide a buffer fullness calculation every cycle, the actual fullness of the buffer is not known continuously every cycle.

The Greenfield et al. encoder does not provide any means to continuously obtain the fullness of the external buffer and does not provide a dynamic buffer level indicator in real-time (every cycle) indicative of the fullness of the external buffer. Further, there is no disclosure in Greenfield et al. that would lead me, as one skilled in the art, to expect that the hardware logic discussed therein would be capable of supporting a continuously obtaining of buffer fullness.

To summarize, the Greenfield et al. real-time encoding system employs use of microcode to update a buffer level indicator. Because microcode is employed, the buffer level signal cannot be returned on a continuous basis (i.e., in real-time), nor every machine cycle. In practice, the buffer level indicator in Greenfield et al. would, for example, be returned approximately once per macroblock. This timing issue resulted in a problem which is identified and addressed by the present application. The Greenfield et al. real-time encoding system inherently has a latency issue which produces an inaccuracy in the FIFO fullness reading because the calculations rely on microcode. Finally, I submit that the final Office Action mischaracterizes the teachings of Greenfield et al. to the extent that it relies upon the "real-time encoding system" characterization to argue that every function within the system inherently continuously occurs on every cycle. Clearly, this is impossible given the nature of software. The real-time encoding (i.e., 30 frames per second) does not equate to a continuous, dynamic indication of buffer fullness, nor more particularly, such a determination thereof every machine cycle.

I declare that all statements for the foregoing Declaration made of my own knowledge are true and that all statements made upon information and belief are believed true and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under section 1001 of Title 18 of the United

States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patent issuing thereon.

Signed by me this 18th day of November, 2002.

Agnes Y. Ngai